APPLICATION FOR UNITED STATES LETTERS PATENT

For

TECHNIQUES TO MANUFACTURE OPTICAL SIGNAL TRANSMITTERS

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TECHNIQUES TO PROVIDE PROGRAMMABLE FINITE IMPULSE RESPONSE FILTERING

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Field

[0001]   The subject matter disclosed herein generally relates to techniques to filter signals.

Description of Related Art

[0002]   Digital domain signal processing is common. Digital signals need to be converted to analog signal format for real world use. Digital-to-analog converters (DAC) convert digital signals to analog format. DACs utilize low-pass filtering before a digital signal is converted to analog format. A finite impulse response (FIR) filter is one efficient approach to implement low-pass filtering. An N-tap FIR filter with coefficients a(k) and input x(n) can have an output y(n) can described by:

$$y(n) = a(0)x(n) + a(1)x(n-1) + a(2)x(n-2) + \ldots a(N-1) \, x(n-N+1),$$

For example, analog coefficients (a(0) ... a(N-1)) can be implemented by providing currents having magnitudes proportional to the coefficient value.

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Brief Description of the Drawings

[0003]   The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

[0004]   FIG. 1 depicts a filter, in accordance with an embodiment of the present invention;

[0005]   FIG. 2 depicts an example of a current mirror set, in accordance with an embodiment of the present invention; and

[0006]   FIG. 3 depicts a system in which some embodiments of the present invention may be used, in accordance with an embodiment of the present invention.

[0007]   Note that use of the same reference numbers in different figures indicates the same or like elements.

Detailed Description

[0008]   In accordance with an embodiment of the present invention, FIG. 1 depicts a filter 100. One implementation of filter 100 may include a shift register 102, bias current source 104, current mirror sets 106-0 to 106-(N-1), and current-to-voltage converter 108. Herein, current mirror set 106 refers to any or all of current mirror sets 106-0 to 106-(N-1).

[0009]   Filter 100 may receive a digital input signal labeled INPUT and provide an analog voltage representation of such digital input signal. For example, filter 100 may be used as an N-

tap FIR filter having programmable coefficients, $a(i)$, where $i = 0$ to $N-1$, as in the relationship described earlier. The magnitude and quantum tunability of each coefficient, $a(i)$, may be independently programmed. Magnitudes of coefficients, $a(i)$, may be based on a filter program (e.g., a rectangular window, hamming window, or hanning window).

[0010]   Shift register 102 may receive digital input signal INPUT. Shift register 102 may output multiple bits, $C_0 \ldots C_{N-1}$. The output of shift register 102 may be initialized to zero. At each increment of a clock signal, shift register 102 may step bits of signal INPUT among output bits. The output bits of shift register 102, $C_0 \ldots C_{N-1}$, may control which of current mirror sets 106-0 to 106-(N-1) provide current to current-to-voltage converter 108. In one implementation, each output bit, C_i, may control whether an associated current conducting switch that couples a current mirror set 106-i to current-to-voltage converter 108 allows current to flow from such current mirror set 106-i to current-to-voltage converter 108. The current provided by all of the current mirror sets 106-0 to 106-(N-1) at any time, t, may be represented in time by the following relationship:

$$I_{sum}(t) = I_0*(C_0(t)) + I_1*(C_1(t)) + \ldots I_{N-1}*(C_{N-1}(t))$$

where

I_0 to I_{N-1} are currents provided by respective current mirror sets 106-0 to

106-(N-1), and

$C_0(t)$ to $C_{N-1}(t)$ are the one/ zero levels of output bits from the shift register 102 as

a function of time t.

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[0011]   FIG. 2 depicts an example of a current mirror set 106-i, in accordance with an embodiment of the present invention. One implementation of current mirror set 106-i may include first current source 202, second current source 204, and control logic and register block 206. Bias current source 104 may provide currents $I_{ref}/16$ and I_{ref} to respective first current source 202 and second current source 204.

[0012]   Each current mirror set 106-i may provide current I_i that represents a coefficient, a(i). The amount of current, I_i, output by each current mirror set 106-i can be independently programmed to be any level and any incremental tunability.

[0013]   Control logic and register block 206 may decode a command (labeled "PROGRAM COMMAND") and provide an "m" bit control signal to control the level of current output by each current mirror set 106-i. In the implementation of FIG. 2, the command is 3-bits and "m" is 8-bits. Other numbers of control bits may be used to control the increments by which the level of current from each current mirror set 106-i can be varied.

[0014]   In one implementation, each current mirror set 106-i may include an integer "m" switches (b_0 ... b_{m-1}) that control whether an individual current source within current mirror set 106-i provides current contribution output from the current mirror set 106-i. In one implementation, first current source 202 may provide a current that is approximately equal to:

$1/16*[b_0/16+b_1/8+b_2/4+b_3/2]*I_{ref}$,

where each of b_0, b_1, b_2, and b_3 are either '0' or '1'.

Second current source 204 may provide a current that is approximately equal to:

$[b_4/16+b_5/8+b_6/4+b_7/2]*I_{ref}$,

where each of b_4, b_5, b_6, and b_7 are either '0' or '1'.

The amount of current (I_i) output by each current mirror set 106-i can be represented by the following equation:

$$I_i = \{1/16*[b_0/16+b_1/8+b_2/4+b_3/2] + [b_4/16+b_5/8+b_6/4+b_7/2]\}*I_{ref}$$

where

$b_0 \ldots b_7$ are an 8-bit input to each current mirror set 106-i

and $b_j = 0$ if the switch is open or 1 if the switch is closed (where j = 0 to 7).

[0015]   Currents from current mirror sets 106-0 to 106-(N-1) may be summed and the sum converted to a voltage to provide an FIR filter response to an input signal. The output voltage, Vout, may be represented by:

$$Vout = Isum*R$$

where R is an impedance (e.g., resistor) value in current-to-voltage conversion.

[0016] FIG. 3 depicts a system 300 in which some embodiments of the present invention may be used. System 300 may include a digital signal source 302, digital-to-analog ("D/A") converter 304, and analog signal receiver 306. System 300 may be used for example in a transmitter device in a communications system. Digital signal source 302 may provide a digital signal to D/A converter 304. Examples of digital signal source 302 include but are not limited to an audio signal source, a video signal source, or communications signal source.

[0017]   D/A converter 304 may utilize some embodiments of the present invention to convert digital signals to analog format. D/A converter 304 may provide an analog version of the digital signal from digital signal source 302 to analog signal receiver 306. Analog signal

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receiver 306 may filter, amplify analog signals, and/or provide sufficient power to drive analog devices (such as speaker or a transmission medium).

Modifications

[0018]　　　The drawings and the forgoing description gave examples of the present invention. The scope of the present invention, however, is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of the invention is at least as broad as given by the following claims.